14. (Amended) A method for producing a semiconductor device according to Claim 12, wherein the step of forming the cylindrical portion on the core and the bottom portion wherein [an] the outer wall of the cylindrical portion is roughened, comprises forming amorphous silicon on said core and said bottom portion; conducting an anisotropic etching to form a side-wall like cylindrical portion at the side of said core and said bottom portion; and roughening an outer surface of said amorphous silicon by forming silicon grains in the outer surface of it to thereby form said cylindrical portion.

REMARKS

At the time of the Office Action dated August 20, 2002, claims 5-18 were pending. Claims 5, 8-12 and 15-18 have been rejected under 35 U.S.C. §112, first paragraph and claims 5-18 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh et al. in view of admitted prior art in the instant application together with DeBoer et al.

Claims 6-8, 10 and 12-14 have been amended, and claims 5 and 11 has been cancelled. Care has been exercised to avoid the introduction of new matters. Claims 6 and 7 have been amended to place the claims in independent form and include all of the limitations recited in independent claim 5, upon which claims 6 and 7 depend, in response to §103(a) rejection. Claim 7 has also been amended to include all the limitation recited in claim 11 in response to §103(a) rejection. Cosmetic amendment has also been made to claims 8 and 10 according to amendment made to claim 6. Claims 6, 7, and 12-14 have also cosmetically been amended for improved clarity.

A clean copy of amended claims 6-8, 10 and 12-14 appears in the Appendix hereto.

Claims 5, 8-12 and 15-18 stand rejected under 35 U.S.C. §112, first paragraph, because the claims purportedly contain subject matter not described in the specification.

As to claims 5 and 12, the Examiner raised an issue as to the limitation "a step of forming an electric conductive film...," saying that applicants claim that the conductive layer comprises amorphous silicon which is a well-known semi-insulative material. The Examiner continued and asked Applicants if doped polycrystalline silicon is claimed.

First, Applicants note that the rejection of claim 5 is rendered moot by cancellation of claim 5. Second, Applicants argue that the specification is presumed enabling. Therefore, the Examiner must provide technical logical reasons upon which to doubt that the specification would not have enabled one having ordinary skill in the art to make and/or use the claimed invention. It is inconceivable that one having ordinary skill in the art would not have been able to fabricate a semiconductor device having a capacitor as the claim describes. The Examiner's questioning does not discharge his burden.

Specifically, the Examiner has not factually established that an amorphous silicon, regardless of how doped, is "semi-insulative" whatever the Examiner means by that expression. At any rate, as the Examiner noted, during roughening, "silicon grains" are formed. The fact that grains are formed means that the amorphous silicon has been converted to polycrystalline silicon, at least at the outer portion. As one having ordinary skill in the art would also have recognized, during fabrication steps subsequent to

pg. 14

formation of the capacitor, elevated temperatures which are employed would convert the amorphous silicon film into polycrystalline silicon. For example U.S. Patent No. 5,866,930 to Saida et al., entitled SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, (copy provided), teaches that amorphous silicon displays electroconductivity in certain circumstances, which enable it to be used for an electrode (see Abstract, column 9, lines 14-24, and column 9, line 66 through column 10, line 3).

Accordingly, the Applicants submit that one having ordinary skill in the art would have no difficulty practicing the claimed invention by guidance from the description, without undue experimentation.

As to the ultimate sentence in the first enumerated paragraph on page 2, Applicants would point out that an ultimate semiconductor device having a capacitor with a roughen amorphous silicon layer is not being claimed. Rather, the claims are directed to a method, which involves roughening the amorphous silicon as disclosed and enabled.

Applicants, therefore, submit that the imposed rejection of claims 5, 8-12 and 15-18 under 35 U.S.C. §112, first paragraph is not viable and, hence, solicit withdrawal thereof.

Claims 5-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hsieh et al. in view of the applicants' admitted prior art and DeBoer et al.

As to claims 5 and 12, the Examiner admitted that Hsieh et al. does not teach the step of forming the lower electrode having a cylindrical shape. The Examiner then cited Applicants' admitted prior art, and stated that it teaches forming a DRAM capacitor structure in which the lower electrode is cylindrical. The Examiner further admitted that

Hsieh et al., in combination with the applicants' admitted prior art, fails to expressly teach roughening the outer wall of the cylindrical storage electrode. Then, the Examiner referred to DeBoer et al. and asserted that it teaches the step of roughening the outer wall of a storage electrode. This rejection is traversed.

Applicants note that the rejection of claim 5 is rendered moot by cancellation of claim 5. Applicants submit that the process claimed in claim 12 is for producing a new, nonobvious semiconductor device which is disclosed in the parent application of this divisional application, now U.S. Patent No. 6,232,628. Specifically, it is not apparent and the Examiner has not identified "a step of forming a dielectric film on said cylindrical storage node comprising said cylindrical portion and said bottom portion within which said core remains." That is, the method is so designed that a core remains within a cylindrical storage node. This results in not only increasing large area of capacitor but also assuring physical strength of a cylindrical storage node. The proposed combination, even if proper, does not teach or suggest the above step of having a core remained within a cylindrical storage node.

Therefore, the Examiner has not established *prima facie* obviousness of the claimed invention. Applicants solicit withdrawal of the rejection of claim 12.

With respect to claims 6-11 and 13-18, the Examiner asserted that the combination of Hsieh et al., the applicants' admitted prior art and DeBoer et al. teaches the step of forming the cylindrical portion on the side of the core and the bottom portion where an outer wall of the cylindrical portion is roughened. The Examiner particularly pointed out that DeBoer teaches the detailed process of forming the cylindrical portion having its outer wall roughened. This rejection is traversed.

Claims 6 and 7 are now in independent form including all of the limitations of claim 5. Claims 6 and 7 include the step of forming the cylindrical portion as well as the step of roughening the outer surface of the cylindrical portion, the features of which are timing of the roughening step.

Whereas the proposed combination of those references might show a concept of roughening the outer surface of a cylindrical storage node, the combination does not teach or suggest timing of the step of roughening treatment as claimed, and its advantage. In claim 6, the surface roughening treatment is conducted right after the formation of the film containing silicon constituting the cylindrical portion. This gives the claimed invention an advantage in that there is no danger of contamination of the film surface, because no step is conducted between the formation of the film and the surface roughening treatment. Considering Hsieh et al. and DeBoer et al., a polysilicon layer 54 should be roughened at the state shown in Fig. 7 of Hsieh, but there is nothing shown in either reference to conduct the roughening treatment to the layer 54 in that state.

On the other hand, in claim 7, the surface roughening treatment is conducted after the formation of the cylindrical portion. As a result, the outer surface at a lower position of the cylindrical portion and near an upper surface of the interlayer insulating film, which has not been roughened in case of claim 6, can be roughened. With respect to this feature of claim 7, DeBoer et al. does not teach or suggest the step of roughening the outer surface at a lower position of the cylindrical portion 6d and near an upper surface of the interlayer insulating film 4. In fact, as shown in Fig. 15 of DeBoer, the layer 86 does not show the result of the roughening treatment. Its exposed surface is smooth. In addition, Applicants submit that DeBoer does not teach or suggest the limitation "the

inner wall of the cylindrical portion having a roughened outer wall is constituted by amorphous silicon," as now recited in claim 7. This is because DeBoer discloses a feature that the amorphous silicon layer is crystallized (column 4, lines 19-20), the feature which is contrary to that recited in claim 7.

Therefore, for the above reason, the proposed combination, even if proper, does not teach or suggest all the limitations of claims 6 and 7. The Examiner has not established *prima facie* obviousness of the claimed invention. Applicants solicit withdrawal of the rejection of claims 6 and 7.

Dependent claims 8-11 and 13-18 would not have also been obvious. If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Accordingly, as claims 6, 7 and 12 are patentable for the reasons set forth above, it is submitted that dependent claims 8-11 and 13-18 which each depend on claim 6, 7 are 12, respectively, also patentable. Applicants specifically submit that as to claim 10, even though the outer wall is crystallized, it is significant that the inner wall is not crystallized and remains to be amorphous. The proposed combination, even if proper, does not teach or suggest the limitation recited in claim 10.

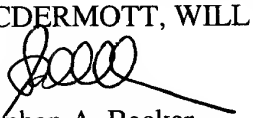
Applicants note that the rejection of claim 11 is rendered moot by cancellation of claim 11. Applicants, therefore, traverse the rejections of those claims and solicits withdrawal thereof.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 15, line 23 as follows:

C1

As shown in Figure 3, the amorphous silicon film 13a remains without discontinuation in the inner wall of the cylindrical portion 6d, and surface of the amorphous silicon film 13a is smooth. The remaining amorphous silicon film 13a is sufficient to keep the physical strength of the cylindrical portion 6b even after the formation of the silicon grains 13b.

Please amend the paragraph beginning at page 19, line 18 as follows:

C2

In the semiconductor device shown in Figure 5, it is impossible for the capacitor 9a to use as an opposing electrode the inner wall of the cylindrical portion 6d and the bottom portion of the cylindrical storage node 6b. However, assuming that the cylindrical storage node 6b is a cylindrical form having a radius (x) of 0.40 μm and the surface area of the outer wall is increased 2.5 times by the surface roughening treatment, the surface area which can be used for the storage node can be increased 1.2 times as large as a case without conducting the surface roughening treatment to the outer wall.

Please amend the paragraph beginning at page 21, line 10 as follows:

C3

Since the core 11a is left in this embodiment, the inner wall of the cylindrical portion 6d and the bottom portion of the storage node 6b can not be used as an opposing electrode. However, the outer wall of the cylindrical portion 6d is roughened, and

accordingly, the surface area of the outer surface as an electrode can be increased as the whole in the cylindrical storage node 6b.

c3

IN THE CLAIMS:

Claims 6-8, 10 and 12-14 now read as follows:

6. (Amended) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises the steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

c4

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that the core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising forming a film containing silicon on said core and said bottom portion; roughening an outer surface of said film containing silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching for patterning to form a side-wall like cylindrical portion at the side of said core and said bottom portion;

removing said core;

forming a dielectric film to cover said cylindrical storage node comprising said cylindrical portion and said bottom portion; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed.

7. (Amended) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises steps of:

C4

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that the core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened, comprising forming amorphous silicon on said core and said bottom portion; conducting an anisotropic etching to form a side-wall like cylindrical portion at the side of said core and said

bottom portion; and roughening an outer surface of said amorphous silicon by forming silicon grains in the outer surface of it to thereby form said cylindrical portion;

removing said core;

forming a dielectric film to cover said cylindrical storage node comprising said cylindrical portion and said bottom portion; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed,

C4 wherein the inner wall of the cylindrical portion having a roughened outer wall is constituted by amorphous silicon.

8. (Amended) A method for producing a semiconductor device according to Claim 6, wherein the roughening of the outer surface of the film containing silicon is selected from the group consisting of a heat treatment with use of silane and a heat treatment in vacuum after a treatment to the outer surface of said film containing silicon with use of hydrofluoric acid, whereby projections and recesses are formed in the outer wall of said amorphous silicon by forming silicon grains in the outer wall.

10. (Amended) A method for producing a semiconductor device according to Claim 8, wherein the inner wall of the cylindrical portion having a roughened outer wall is constituted by said film containing silicon, said film containing silicon including amorphous silicon.

C5

12. (Amended) A method for producing a semiconductor device having a cylindrical storage node comprising a bottom portion and a cylindrical portion which surrounds an outer circumference of said bottom portion and extends upward, which comprises steps of:

forming a contact hole which penetrates an interlayer insulating film formed on a semiconductor substrate;

forming an electric conductive film on said interlayer insulating film whereby said contact hole is filled to obtain a contact to said substrate;

forming an insulating film on said electric conductive film;

C6 patterning by an anisotropic etching said insulating film and said electric conductive film to form a configuration corresponding to said cylindrical portion so that the core and the bottom portion of said cylindrical portion are formed;

forming the cylindrical portion on the side of said core and said bottom portion wherein an outer wall of said cylindrical portion is roughened;

forming a dielectric film on said cylindrical storage node comprising said cylindrical portion and said bottom portion within which said core remains; and

forming a cell plate on said dielectric film, whereby a capacitor constituted by said cylindrical storage node, said dielectric film and said cell plate is formed.

13. (Amended) A method for producing a semiconductor device according to Claim 12, wherein the step of forming the cylindrical portion on the side of the core and the bottom portion wherein the outer wall of the cylindrical portion is roughened, comprises forming amorphous silicon on said core and said bottom portion; roughening

an outer surface of said amorphous silicon by forming silicon grains in the outer surface of it; and conducting an anisotropic etching for patterning to form a side-wall like cylindrical portion at the side of said core and said bottom portion.

14. (Amended) A method for producing a semiconductor device according to Claim 12, wherein the step of forming the cylindrical portion on the core and the bottom portion wherein the outer wall of the cylindrical portion is roughened, comprises forming amorphous silicon on said core and said bottom portion; conducting an anisotropic etching to form a side-wall like cylindrical portion at the side of said core and said bottom portion; and roughening an outer surface of said amorphous silicon by forming silicon grains in the outer surface of it to thereby form said cylindrical portion.